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MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICES

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SEMICONDUCTOR DEVICE MANUFACTURING METHOD

[Handotaisochi no seizohoho]

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[There are no amendments to this patent.]

Claim

1. A semiconductor device manufacturing method characterized in that it includes:

(a) a process in which an amorphous material layer which mainly consists of silicon is formed upon insulating amorphous material,

(b) a process in which a metal layer is formed upon the said amorphous material layer for pattern formation,

(c) a process in which crystal nuclei are grown in areas in which the said amorphous material layer makes contact with the said metal layer by heat treatment, for example,

(d) a process in which the said amorphous material layer is crystal grown through a heat treatment, for example, by using the aforementioned crystal nuclei as seeds, and

(e) a process in which a semiconductor element is formed in the silicon layer which is crystal grown.

Detailed explanation of the invention

Field of industrial application

The present invention concerns a manufacturing method for semiconductor devices, in particular, it concerns a manufacturing method for semiconductor devices in which a monocrystalline semiconductor film is selectively formed upon insulating amorphous material.

Conventional technology

Attempts have been made to form a high-performance semiconductor element upon an insulating amorphous substrate, such as glass and quartz, for example, and an insulating amorphous layer, such as SiO_2, for example.

As the need for large, high-definition liquid crystal display panels with high-speed, high-definition contact-type image sensors, and three-dimensional ICs, for example, has increased in recent years, so has the expectation of realizing the aforementioned high-performance semiconductor elements upon an insulating amorphous material.

Using the formation of a thin film transistor (TFT) upon insulating amorphous material as an example, the following is being examined: (1) TFT using amorphous silicon which is formed by the plasma CVD method, for example, as the element material; (2) TFT using polycrystalline silicon which is formed by the CVD method, for example, as the element material; and (3) TFT using monocrystalline silicon which is formed by the fusion recrystallization method, for example, as the element material.

However, of these TFTs, with respect to TFTs using amorphous silicon and polycrystalline silicon as the element materials, the mobility of the carriers with applied electric field of these types of TFTs is dramatically lower than when monocrystalline silicon was used as the element material (amorphous silicon TFT < 1 $cm^2/V \cdot sec$ and monocrystalline silicon TFT ≈ 10 $cm^2/V \cdot sec$), therefore, attainment of a high-performance TFT was difficult.

Also, the fusion recrystallization method using a laser beam, for example, cannot yet be considered a sufficiently developed technology. Moreover, the technical difficulty is particularly great when it is necessary for an element to be formed for a large area as in a liquid crystal display panel, for example.

Therefore, a method in which polycrystalline silicon having a large particle diameter can be solid grown has received much attention and its research has advanced to the point where the technique is an easy yet practical method to form a high-performance semiconductor element on an insulating amorphous material (Thin Solid Films 100 (1983) p. 227, JJAP Vol. 25 No. 2 (1986) p.L121).

Problems to be solved by the present invention

However, sufficient control of the particle diameter of the polycrystalline silicon and the position at which the crystal grain boundary is present was difficult in the conventional technology. Accordingly, even though polycrystalline silicon with a large particle diameter can be tentatively formed, there was a drastic difference between the characteristics of a TFT which is formed with the crystal grain and a TFT with the channel region of the TFT located at the crystal grain boundary. Therefore, serious problems occurred such as the operating speed of scanning circuits constructed from TFT being controlled by the poor characteristics of TFTs located at the crystal grain boundary, and the circuit not operating under worst care conditions, for example.

Therefore, the present invention provides a manufacturing method in which the position of the crystal grain boundary is controlled and a semiconductor element is selectively formed in a crystal region.

Means to solve the problems

The semiconductor device manufacturing method of the present invention is characterized in that it includes:

(a) a process in which an amorphous material layer which mainly consists of silicon is formed upon insulating amorphous material,

(b) a process in which a metal layer is formed upon the said amorphous material layer for pattern formation,

(c) a process in which crystal nuclei are grown in areas at which the said amorphous material layer makes contact with the said metal layer by a heat treatment, for example,

(d) a process in which the said amorphous material layer is crystal grown through a heat treatment, for example, by using the aforementioned crystal nuclei as seeds, and

(e) a process in which semiconductor elements are formed in the silicon layer which is crystal grown.

Application examples

Figure 1 shows one example of manufacturing process diagrams of a semiconductor device in an application example of the present invention. An example in which a thin film transistor (TFT) is formed as a semiconductor element is used in Figure 1.

In Figure 1, (A) indicates a process in which an amorphous material layer (102) which consists mainly of silicon is formed on insulating amorphous material (101), such as an insulating amorphous substrate consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example. Methods for forming the said amorphous material layer include forming an amorphous silicon film by plasma CVD, vapor deposition, EB deposition, MBE, sputtering, and CVD, for example; methods in which monocrystalline silicon or polycrystalline silicon, for example, is first formed include plasma CVD, CVD, vapor deposition, EB deposition, MBE, and sputtering, for example, and an element, such as Si, Ar, B, P, He, Ne, Kr, and H, for example, is ion implanted in order to noncrystallize the said monocrystalline silicon or polycrystalline silicon, for example.

(B) indicates a process in which a metal layer (103) is formed upon the said amorphous material layer (102), the said metal layer is eliminated while leaving sections which become seed regions (104), and crystal nuclei which become seeds are formed in areas in which the said amorphous material layer (102) makes contact with the metal layer (103) through heat treatment, for example. Using Al as the metal layer, for example, the temperature of the amorphous silicon which makes contact with the said metal layer (103) is lower than other areas, and crystal nuclei can easily be generated in a short period of time. Accordingly, since heat treatment is processed at the temperature and time at which crystal nuclei are not generated in areas which do make contact with the metal layer, crystal growth can be selectively induced from the seed regions (104). In a specific

example, since heat treatment is processed at approximately 200°C to 450°C for approximately 15 min to 2 h after vapor-depositing Al, for example and pattern forming it, crystal nuclei are formed near the interface between the metal layer and the amorphous silicon layer, and crystal growth starts. The metal layer (Al) (103) is successively removed with phosphoric acid, for example, through etching. The reason for eliminating the metal layer is to prevent an abnormal diffusion of the metal into the amorphous silicon (particularly into the element forming region) during heat treatment at high temperature which successively takes place. The aforementioned abnormal diffusion can also be prevented by establishing the film thickness of the metal layer, such as Al, for example, at least at the same or less than the film thickness of the amorphous silicon layer. For example, the abnormal diffusion can be reduced by using a metal layer of approximately 100-500 Å or less on an amorphous silicon layer of 200-1000 Å.

The heat treatment temperature for forming crystal nuclei has a different optimum value accordingly to the film forming method for amorphous silicon. For example, crystal nuclei are formed at a relatively low temperature of approximately 200-350°C when the amorphous silicon which is formed by the plasma CVD method is used. Accordingly, there is merit in forming crystal nuclei in the seed regions through low temperature heat treatment since it is difficult to generate crystal nuclei in areas other than the seed regions.

(C) indicates a process in which the said amorphous material layer (102) is selectively crystal grown through heat treatment, for example, using the said seed regions (104) as starting

points. The heat treatment temperature is approximately 550-650°C, and heat treatment is applied for approximately 20-30 h.

(D) indicates a process in which a semiconductor element is formed in the crystal grown silicon layer (105). TFT is formed as a semiconductor element in the example in Figure 1 (D). In the figure, (106) is a gate electrode, (107) is a source-drain region, (108) is a gate insulating film, (109) is a layer insulating film, (110) is a contact hole, and (111) is wiring. As one example of the TFT formation method, the silicon layer (105) is patterned and a gate insulating film is formed. The said gate insulating film can be formed by a method using the thermal oxidation method (high temperature process) or by a method at a low temperature of less than 600°C by the CVD method or the plasma CVD method, for example, (low temperature process). Inexpensive glass substrates can be used when the low-temperature process is used, therefore, semiconductor devices, such as large liquid crystal display panels and contact type image sensors, for example, can be fabricated at low cost, and also when forming a three-dimensional IC, for example, a semiconductor element can be formed at the upper layer section without negatively affecting the element at the lower layer section (diffusion of impurities, for example). The gate electrode is successively formed, and the source-drain region is formed by ion injection, thermal diffusion, or plasma doping, for example, and the layer insulating film is formed by the CVD, sputtering, or plasma CVD, for example. Furthermore, a contact hole is formed at the said layer insulating film for forming wiring, and TFT is formed.

The mobility of the carriers with applied electric field of the low temperature processed TFT (n-channel) manufactured by the manufacturing method for semiconductor devices based on the present invention is 200-350 $cm^2/V \cdot sec$, and a high-performance TFT was formed on a glass substrate. This is the result of the selective crystal growth with satisfactory processability by the manufacturing method of the present invention. Furthermore, the defect density is reduced and the aforementioned mobility of the carriers with applied electric field further improves if the process in which the semiconductor element is exposed to a plasma atmosphere formed from a gas, such as hydrogen gas or ammonia gas, is included in the aforementioned TFT forming process.

Figures 2 and 3 indicate another example of manufacturing process diagrams of a semiconductor device in an application example of the present invention. Figure 2 indicates cross-sectional diagrams, and Figure 3 indicates top view diagrams.

In Figures 2 and 3, (A) indicates a process in which an amorphous material layer (202) which consists mainly of silicon is formed on insulating amorphous material (201), such as an insulating amorphous substrate consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example. Methods for forming the said amorphous material layer include forming the amorphous silicon by plasma CVD, vapor deposition, EB deposition, MBE, sputtering, and CVD, for example, a method in which monocrystalline silicon or polycrystalline silicon, for example, is first formed by plasma CVD, CVD, vapor deposition, EB deposition, MBE, and sputtering,

for example, and an element, such as Si, Ar, B, P, He, Ne, Kr, and H, for example, is ion implanted in order to noncrystallize the said monocrystalline silicon or polycrystalline silicon, for example.

(B) indicates a process in which a metal layer (203) is formed upon the said amorphous material layer (202), the said metal layer is removed while leaving sections which become seed regions (204), and crystal nuclei which become seeds are formed in an area in which the said amorphous material layer (202) makes contact with the metal layer (203) through heat treatment, for example, and the said amorphous material layer (202) is successively patterned to the desired form. Also, the amorphous material layer can also be patterned before growing the seed regions. Using Al as the metal layer in an example, as described above, the temperature of the amorphous silicon that makes contact with the said metal layer (203) is lower than other areas, and crystal nuclei can easily be generated in a short period of time. Accordingly, since heat treatment is applied at the temperature and time at which crystal nuclei are not generated in areas which do not make contact with the metal layer, crystal growth can be selectively induced from the seed regions. In a specific example, since heat treatment is applied at approximately 200-450°C for approximately 15 min to 2 h, crystal nuclei are formed near the interface between the metal layer and the amorphous silicon layer, and crystal growth starts. The metal layer (Al) (203) is successively removed with phosphoric acid, for example, through etching. As described above, the reason for removing the metal layer is to prevent the abnormal diffusion of the metal into the amorphous silicon

(particularly into the element forming region) during heat treatment at a high temperature which subsequently takes place. The heat treatment temperature for forming crystal nuclei has a different optimum value according to the film forming method for amorphous silicon. For example, crystal nuclei are formed at a relatively low temperature of approximately 200-350°C when the amorphous silicon which is formed by the plasma CVD method is used. Accordingly, there is merit in forming crystal nuclei in the seed regions through a low temperature heat treatment since it is difficult to generate crystal nuclei in areas other than the seed regions.

The amorphous silicon layer is patterned to a specific form. Figure 2 indicates an example in which the aforementioned amorphous silicon layer is patterned to a form which includes island regions (205) and connecting regions (206) which connect the said island region (205) to the said seed region (204).

(C) indicates a process in which the said amorphous material layer (202) is selectively crystal grown through heat treatment, for example, using the said seed regions (204) as starting points. The heat treatment temperature is approximately 550-650°C, and heat treatment is applied for approximately 20-30 h.

By patterning the amorphous silicon layer to include island regions (205) and connecting regions (206) as described above, even when multiple crystal nuclei are formed in the seed regions, any of the connecting regions which are superior (such as a fast crystal growth speed or early generation of crystal nuclei, for example) are selected for fast crystal growth, and the island regions are monocrystallized. Figure 4 indicates a pattern

diagram of the said crystal growth. In Figure 4, (401) is the island region, (402) is the connecting region, (403) is the seed region, and (404) and (405) indicate crystal grains.

As indicated in the pattern diagram of the crystal growth in Figure 5, the location of the existence of the crystal grain boundary can be significantly limited even when monocrystalline growth is not selected in the connecting region. In Figure 5, (501) is the island region, (502) is the connecting region, (503) is the seed region, (504) is a location at which the probability of the existence of the crystal grain boundary is high, and (505) are the areas in which the probability of the presence of the crystal grain boundary is practically zero. (506) is a region between both (gray zone). Accordingly, when using a MOS transistor and TFT as examples of the semiconductor element, a significant variation in element characteristics by the crystal grain boundary can be eliminated by arranging the element so that the channel region of the said element is arranged within the region (405).

(D) indicates a process in which a semiconductor element is formed at the crystal grown island regions (205). TFT is formed as a semiconductor element in the example in Figure 2 (D). In the figure, (207) is a gate electrode, (208) is a source-drain region, (209) is a gate insulating film, (210) is a layer insulating film, (211) is a contact hole, and (212) is wiring. The method of formation of TFT can be the same method as in the application example of Figure 1. As described above, the variation of element characteristics by the crystal grain boundary can be eliminated by arranging the channel region (213) of the TFT in a region at which the probability of the existence

of the crystal grain boundary is practically zero, and the yield significantly improved.

With respect to the pattern of the amorphous silicon layer, various other forms can be considered besides the shapes indicated in Figure 2. For example, Figures 6-8 indicate examples of top view diagrams of connecting regions in the application examples of the present invention. In Figures 6-8, (601), (701), and (801) are seed regions, (602), (702), and (802) are island regions, (603), (703), and (803) are connecting regions, (604) and (605), (704) and (705), and (804) and (805) are crystal grains. The selection of crystal growth can be attained more completely by devising the form of the connecting region, such as by tapering the width of the connecting region and providing a region of narrow width (706), for example. Polycrystal nuclei are easily generated in the seed region particularly in the seed formation method using the metallic film based on the present invention; therefore, the aforementioned selection of the crystal growth effectively brings about a drastic improvement in the yield. Also, the heat treatment time is shortened by increasing crystal growth speed by approximately 10 times by doping with a concentration of approximately $10^{[illegible]}$-$10^{[illegible]}cm^{-3}$ with such impurities as P (phosphorus), for example, in the connecting region, for example, and it is particularly effective when more widely crystallizing the island region, which is the region in which the element is to be formed.

Examples in which Al was used as the metal layer were used in the application examples in Figures 1-3; however, the present invention is not so limited. For example, Al alloys, such as

Al-Si, for example, metals, such as Cr, Ni, Mo, W, Au, Pt, and Ti, for example, and their alloys can be used as the said metal layer. In some cases, crystal nuclei are easily generated when an alloy of Si and a metal, such as Al-Si, for example, is used. Using Al-Si as an example, crystal nuclei are easily and evenly generated when the Si content is less than approximately 0.5 wt% (it is difficult to generate crystal nuclei unless a heat treatment at a higher temperature is applied when the Si content is greater than the aforementioned value).

In the application examples, the metal layer was formed on the amorphous silicon layer; however, the order of lamination can be reversed. However, problems, such as the inability to remove the metal layer before heat treatment and covering areas of the metal layer with step differences with the amorphous silicon layer, for example, occur when the amorphous silicon layer is formed above the metal layer.

Besides the TFTs indicated in the application examples, the present invention can also be applied in general to insulated gate semiconductors, and it can also be applied in general to semiconductor elements such as photoelectronic transducers, bipolar transistors, field-effect transistors, solar batteries, and optical sensors, for example, and it becomes a very effective manufacturing method.

Effects of the present invention

As described above, in the present invention monocrystalline silicon, for example, is selectively grown upon insulating amorphous material, such as an insulating amorphous substrate

consisting of glass and quartz, for example, or an insulating amorphous material layer consisting of SiO_2, for example, and the position at which the crystal grain boundary should be present can be controlled. As a result, it becomes possible to selectively form a semiconductor element in a crystallized region. A high-performance semiconductor element which is equivalent to a semiconductor element that is formed on a Si wafer can be formed on the insulating amorphous material of the present invention, and large, high-definition liquid crystal display panels high-speed high-definition contact type image sensors, and three-dimensional ICs, for example, can be easily formed.

Furthermore, unlike the fusion recrystallization method, low temperature heat treatment, which is approximately 650°C at most, is only auxiliary in the present invention. As a result, there are such merits as (1) the ability to use inexpensive glass substrates as the substrate and (2) the ability to form a semiconductor element at the upper layer section without negatively affecting (diffusion of impurities, for example) the element at the lower layer section in the three-dimensional ICs, for example.

Besides the TFTs indicated in the application examples, the present invention can also be applied in general to insulated gate semiconductors, and it can become a very effective manufacturing method when forming semiconductor elements such as photoelectronic transducers, bipolar transistors; field-effect transistors, solar batteries, and optical sensors, for example, upon the insulating material.

Brief explanation of the figures

Figure 1 (a)-(d) are diagrams indicating manufacturing processes for a semiconductor device in an application example of the present invention.

Figure 2 (a)-(d) and Figure 3 (a)-(d) indicate a manufacturing method for a semiconductor device in an application example of the present invention, Figure 2 indicates cross sectional diagrams, and Figure 3 indicates top views.

Figure 4 and Figure 5 are pattern diagrams of the crystal growth.

Figure 6-8 are top views of the connecting regions in the application examples of the present invention.

101, 201···insulating amorphous material, 102, 202···amorphous material layer, 103, 203···metal layer, 104, 204···seed region, 106, 207···gate electrode, 107, 208···source-drain region, 108, 209···gate insulating film, 109, 210···layer insulating film, 110, 211···contact hole, 111, 212···wiring, 401 501, 602, 702, and 802···island region, 402, 502, 603, 703, and 803···connecting region, and 403, 503, 601, 701, and 801···seed region.

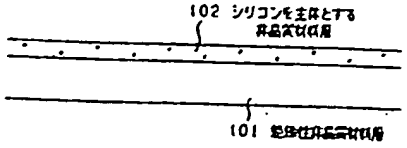


Figure 1 (a)

Key: 101 Insulating amorphous material layer
102 Amorphous material layer mainly consisting of silicon

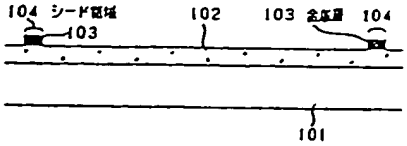


Figure 1 (b)

Key: 103 Metal layer
104 Seed region

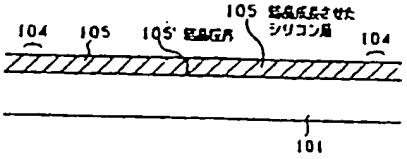


Figure 1 (c)

Key: 105 Crystallized and grown silicon layer
105′ Crystal grain boundary

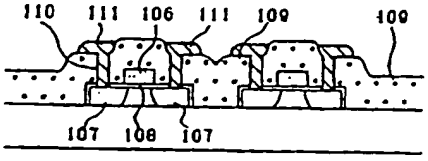


Figure 1 (d)

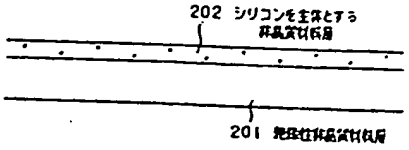


Figure 2 (a)

Key: 201 Insulating amorphous material layer
202 Amorphous material layer mainly consisting of silicon

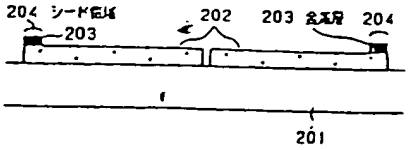


Figure 2 (b)

Key: 203 Metal layer
204 Seed region

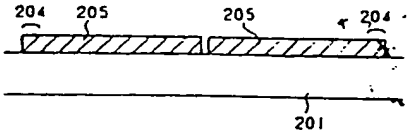


Figure 2 (c)

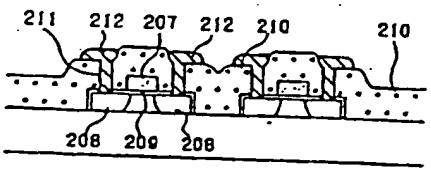


Figure 2 (d)

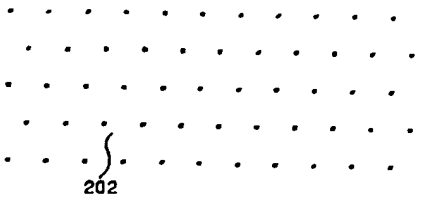


Figure 3 (a)

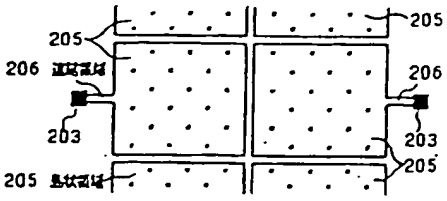


Figure 3 (b)

Key: 205 Island region
206 Connecting region

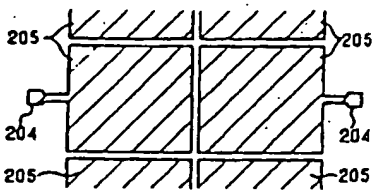


Figure 3 (c)

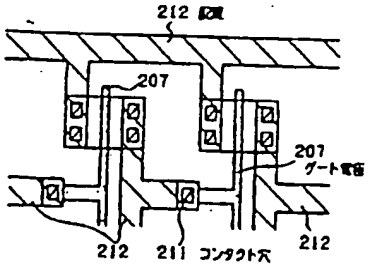


Figure 3 (d)

Key: 207 Gate electrode
211 Contact hole
212 Wiring

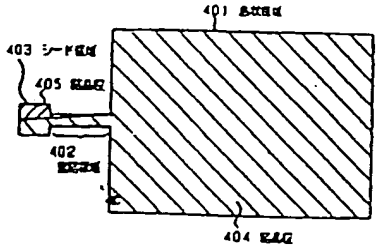


Figure 4

Key: 401 Island region
402 Connecting region
403 Seed region
404 Crystal grain
405 Crystal grain

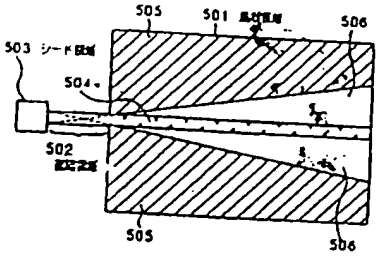


Figure 5

Key: 501 Island region
502 Connecting region
503 Seed region

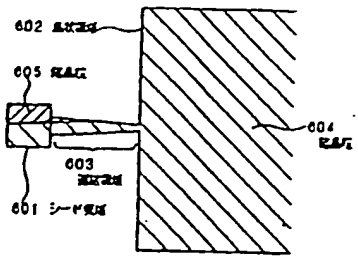


Figure 6

Key: 601 Seed region
602 Island region
603 Connecting region
604 Crystal grain
605 Crystal grain

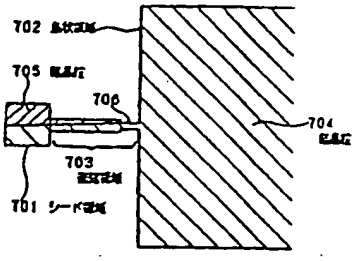


Figure 7

Key: 701 Seed region
702 Island region
703 Connecting region
704 Crystal grain
705 Crystal grain

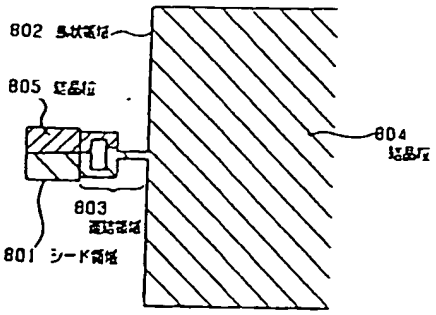


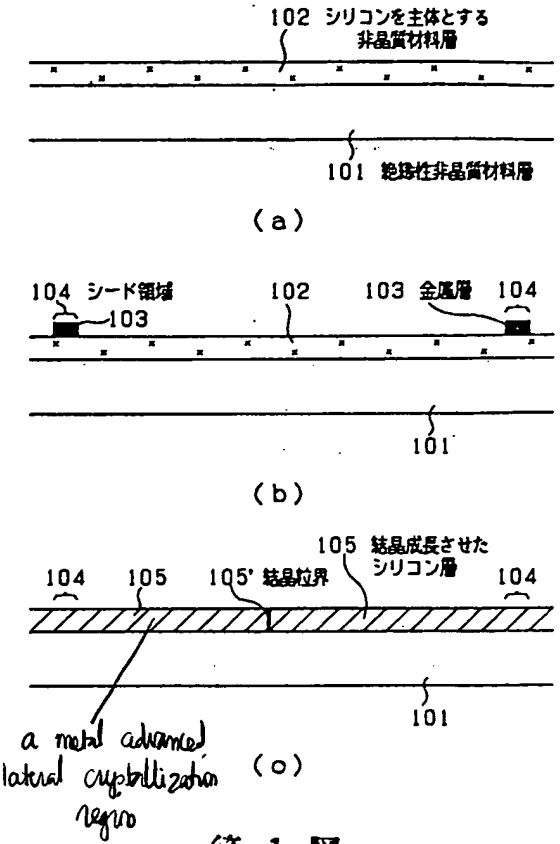
Figure 8

Key: 801 Seed region
802 Island region
803 Connecting region
804 Crystal grain
805 Crystal grain

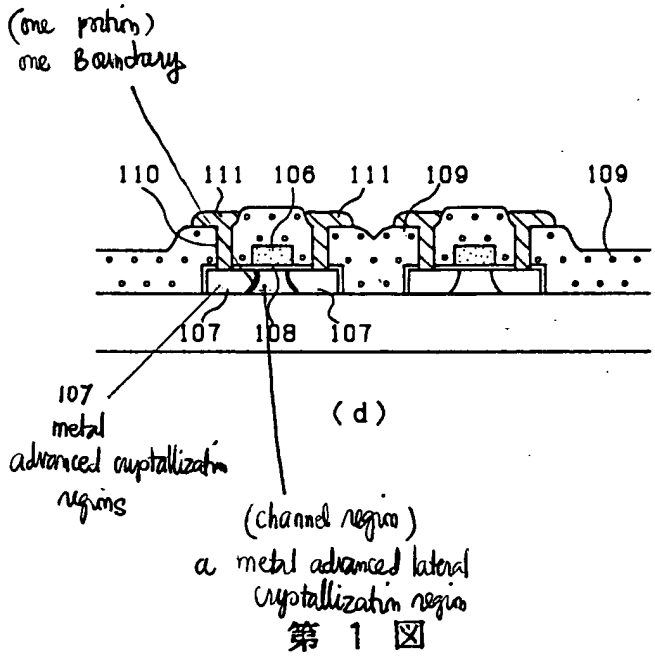
１０３、２０３・・・金属層
１０４、２０４・・・シード領域
１０６、２０７・・・ゲート電極
１０７、２０８・・・ソース・ドレイン領域
１０８、２０９・・・ゲート絶縁膜
１０９、２１０・・・層間絶縁膜
１１０、２１１・・・コンタクト穴
１１１、２１２・・・配線
４０１、５０１、６０２、７０２、８０２
・・・島状領域
４０２、５０２、６０３、７０３、８０３
・・・連結領域
４０３、５０３、６０１、７０１、８０１
・・・シード領域

以　上

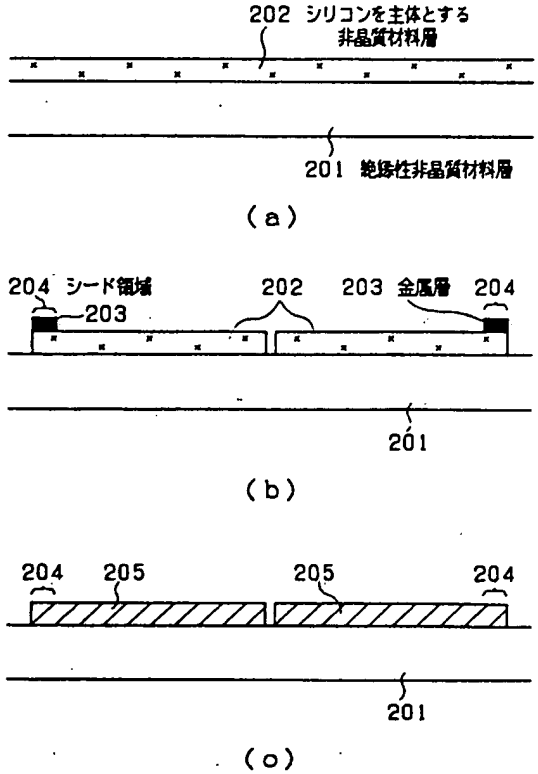
出願人　セイコーエプソン株式会社
代理人　弁理士　上　柳　雅　誉（他１名）



第 1 図



第 1 図



第 2 図